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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/820,765	04/09/2004	Shu-Jung Ma	3183-66	8816

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EXAMINER	
GEBREMARIAM, SAMUEL A	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 02/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/820,765	MA, SHU-JUNG	
	Examiner	Art Unit	
	Samuel A. Gebremariam	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 April 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: page 1, line 25, the word "prepreg" appears to be a typographical error; throughout the specification, the word "showed" appears to be grammatically incorrect. Appropriate correction is required.

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 3-11 and 13-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Kirkman, US patent No. 6,064,113.

Regarding claim 1, Kirkman, teaches (figs. 2, 3 and 4) a package substrate (40) for improving electrical performance comprising: a first insulating layer having a top surface and a bottom surface; a plurality of groups of inner fingers (66 and refer to col. 6, lines 16-30) formed on the top surface of the first insulating layer (the upper layer 42) for electrically connecting to a chip (62); a plurality of outer fingers (68 and refer to col. 6, lines 16-30) formed on the top surface of the first insulating layer (42) for electrically

connecting to the chip (62); a plurality of outer through holes (through holes to the right of 68 and also refer to fig. 4) formed through the first insulating layer and electrically connected to the corresponding outer fingers (68); a plurality of inner through holes through holes (through holes to the left of 66 and also refer to fig. 4) formed through the first insulating layer and electrically connected to the corresponding inner fingers (66); and a ground/power layer (82 or 84) disposed on the bottom surface of the first insulating layer, wherein the ground/power layer has a plurality of openings (region where the ground layer is shown not contacting via 76, fig. 3 and also refer to fig. 4), and the inner through holes are crowded in groups (group of vias in fig. 4) to pass through the openings which are electrically isolated from the ground/power layer (layer 82 is isolated from via 76 or inner through hole).

Regarding claim 3, Kirkman teaches the entire claimed structure of claim 1 above including the ground/power layer between two adjacent openings is in strip shape (ground/power layer is planar therefore it has a strip shape between adjacent openings).

Regarding claim 4, Kirkman teaches the entire claimed structure of claim 1 above including each group of inner through holes pass through the corresponding openings and arranged in grid array (refer to figs. 3 and 4).

Regarding claim 5, Kirkman teaches the entire claimed structure of claim 1 above including the top surface of the first insulating (42) layer includes a chip-attaching region (region where 62 sits, fig. 3).

Regarding claim 6, Kirkman teaches the entire claimed structure of claim 1 above including the openings are radially oriented to the chip-attaching region (refer to fig. 4).

Regarding claim 7, Kirkman teaches the entire claimed structure of claims 1 and 5 above including a metal ring (46) formed on the top surface of the first insulating layer between the chip-attaching region and the inner fingers.

Regarding claim 8, Kirkman teaches the entire claimed structure of claims 1 and 5 above including a second insulating layer (42 the middle layer) formed on the bottom surface of the first insulating layer to sandwich the ground/power layer (refer to fig. 3).

Regarding claim 9, Kirkman teaches the entire claimed structure of claims 1 and 8 above including another ground/power (84) layer on the bottom surface of the second insulating layer.

Regarding claims 10-11 and 13-18 Kirkman teaches (figs. 2, 3 and 4) the entire claimed structure of claims 1 and 3-9 above including a package substrate (40) for improving electrical performance comprising: a first insulating layer (upper layer 42) having a top surface and a bottom surface; a plurality of inner fingers (66 and refer to col. 6, lines 16-30) formed on the top surface of the first insulating layer for electrically connecting a chip (62); a plurality of outer fingers (68 and refer to col. 6, lines 16-30) formed on the top surface of the first insulating layer for electrically connecting the chip (62); a plurality of outer through holes (through holes to the right of 68 and also refer to fig. 4) formed through the first insulating layer and electrically connected with corresponding outer fingers (68); a plurality of inner through holes (through holes to the left of 66 and also refer to fig. 4) formed through the first insulating layer and electrically connected with corresponding inner fingers (66); and a first ground/power layer (82) disposed on the bottom surface of the first insulating layer (bottom surface of upper

layer 42), wherein the first ground /power layer has a plurality of openings (region where the ground layer is shown not contacting via 76, fig. 3 and also refer to fig. 4), at least one of the inner through holes (76) passes through each opening with electrical isolation from the first ground/power layer in a manner that the openings are crowded in groups for improving electrical performance (refer to the abstract).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5. Claims 2 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kirkman.

Regarding claims 2 and 12, Kirkman teaches substantially the entire claimed structure of claims 1 and 10 above except explicitly stating that a distance between the two adjacent openings is not less than 0.2mm.

Parameters such as width and thickness in the art of semiconductor manufacturing process are subject to routine experimentation and optimization to achieve the desired device characteristic during fabrication.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to adjust the distance between the two adjacent openings as claimed in order to stabilize signal path impedances.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. References B and C are cited as being related to semiconductor device packaging.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Samuel A Gebremariam whose telephone number is (571) 272-1653. The examiner can normally be reached on 8:00am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on (571) 272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SAG
February 2, 2005

EDDIE LEE
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